Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	268417	(damascene dual adj damascene trench hole via groove recess opening) with (dielectric insulat$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:56
L2	101593	1 and (damascene dual adj damascene trench hole via groove recess opening) with (wafer substrate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:57
L3	15811	2 and (damascene dual adj damascene trench hole via groove recess opening) with (barrier liner linning seed)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:40
L4	10505	3 and (damascene dual adj damascene trench hole via groove recess opening) with (metal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:41
L5	3609	4 and (damascene dual adj damascene trench hole via groove recess opening) with (inter adj layer interlayer 'ILD')	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:42
L6	1977	5 and (damascene dual adj damascene trench hole via groove recess opening) with (copper "Cu")	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:51
L7	1977	6 and (damascene dual adj damascene trench hole via groove recess opening) with (conduct$3 metal$4 copper "Cu")	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:56
L8	1977	7 and (damascene dual adj damascene trench hole via groove recess opening conduct$3 metal$4 copper "Cu")	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:55
L9	618	8 and (damascene dual adj damascene trench hole via groove recess opening) with (anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:01

L10	152	9 and (damascene dual adj damascene trench hole via groove recess opening) with (etch$4 near3 stop)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 13:59
L11	476	9 and ((inter adj layer interlayer 'ILD' dielectric insulat$3)) with (anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:58
L12	3	11 and ((inter adj layer interlayer 'ILD' dielectric insulat$3)) with (degas)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:02
L13	80	(inter adj layer interlayer 'ILD' dielectric insulat$3) with (degas)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:54
L14	61	13 and ((inter adj layer interlayer 'ILD' dielectric insulat$3)) with (anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:14
L15	61	14 and (inter adj layer interlayer 'ILD' dielectric insulat$3 anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:15
L16	49	15 and (barrier seed line linning) and (inter adj layer interlayer 'ILD' dielectric insulat$3 anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:16
L17	9908	(inter adj layer interlayer 'ILD' dielectric insulat$3) with (degas degased degassing bake$2 baking)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:58
L18	3552	17 and (damascene dual adj damascene trench hole via groove recess opening) with (dielectric insulat$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:56
L19	1842	18 and (damascene dual adj damascene trench hole via groove recess opening) with (wafer substrate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:57
L20	1050	19 and ((inter adj layer interlayer 'ILD' dielectric insulat$3)) with (anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:57

L21	1050	20 and ((inter adj layer interlayer 'ILD' dielectric insulat$3)) with (anneal$4 heat$3 thermal$4)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:58
L22	110	21 and (inter adj layer interlayer 'ILD' dielectric insulat$3) with (degas degased degassing)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/07/21 14:58